REMARKS

The notice of allowable subject matter in Claims 2-4, 7-9 and 12-14 at the top of page 5 of the outstanding Office Action is gratefully appreciated. (The number 24 appears to be a typographical error since only 14 claims were originally filed.) However, in view of the foregoing amendments and the discussion to follow, it is respectfully submitted that the each of the originally presented Claims 1-14 as amended above, as well as each of newly added Claims 15-27, defines subject matter which is not disclosed or suggested by the prior art relied upon in the outstanding Office Action and is, therefore, patentable. Reconsideration of this application in light of the foregoing amendments and following remarks is, accordingly, earnestly solicited.

The rejection of Claims 1-14, under the provisions of the second paragraph of 35 U.S.C. § 112, for the reasons set forth at the top of page 2 of the outstanding Office Action, is respectfully traversed.

The initial allegation of indefiniteness is based upon the inference that it is not clear whether Claims 1, 5 and 10 read upon the prior art of Figure 1, Figure 2, or on both Figures 1 and 2. In fact, the claims recite circuitry which is found in both figures. Attention is directed to the paragraph bridging pages 4 and 5 of the present specification, which indicates that Figure 2 shows an embodiment of the over-voltage protection scheme according to the present invention, which is incorporated as an augmentation to the driver circuitry 2 of the circuitry of Figure 1. The control circuit 10 is operative to perform the functionality of the control circuit 1 of Figure 1 and incorporates combinational logic and flip-flops that implement the over-voltage protection control circuitry subsequently described. In other words, Figure 2 particularly illustrates the present invention and does not repeat the upstream end of Figure 1, in order to avoid unnecessary duplication of the drawings. Withdrawal of the initial objection to Claims 1, 5 and 10 is, accordingly, earnestly solicited.

The objection to the apparent confusion between the phrase "an output voltage terminal" and the phrase "an output node" is well taken. Each of the independent claims has been amended, where appropriate, to insure consistency of terminology. The claims currently refer to "an output node" rather than "an output voltage terminal". Withdrawal of the remaining rejection under 35 U.S.C. § 112 is, accordingly, earnestly solicited.

Applicants have also made minor additional amendments in the claims to insure consistency of terminology throughout.

Before discussing the shortcomings of the prior art relied upon in the rejection of Claims 1, 5, 6, 10 and 11, under the provisions of 35 U.S.C. § 102, the present invention will be briefly reviewed, in order that differences between the US patent to Holt et al 6,731,486 and the claims for which patent protection is sought, including the amended claims and newly added claims, may be more readily appreciated.

As is described in the initial portion of the present specification, a critical aspect of the functionality of the switching circuit that drives the output power supply rail of the regulated power supply is the need to avoid an over-voltage condition that can result from a short circuit in the upper switched electronic device. If a short circuit condition anomaly exists in the upper switching device and that anomaly is not detected and corrected before completing power up, the common node will suffer an over-voltage condition, which may propagate therefrom and damage downstream circuitry.

The present invention circumvents this problem, by monitoring the voltage at the common node between the upper and lower switched FETs during initial power up of the system. Monitoring of the voltage at the common node in accordance with the present invention is readily effected by way of an over-voltage protection resistor 50, shown being connected between the common or phase node 5 and the control or gate input to the lower FET 4.

As is described in paragraphs 16 and 17 of the present specification, during initial power up, if there were a short-circuit condition across the upper FET 3, the voltage at the phase node would ramp up towards the power supply rail. As the common node voltage increases, resistor 50 couples this voltage to the control input or gate of the lower FET 4. When the voltage reaches the threshold of the lower FET, FET 4 turns on, thereby providing an over-voltage by-pass path to ground. When this occurs, voltage error amplifier circuitry within the power supply's control circuitry will detect a short circuit to ground at the power supply output and take action to shut down the operation of the converter to prevent potential damage to powered components. Namely, the effectively immediate by-pass of a potential over-voltage condition to ground in accordance with the invention successfully prevents an excessive voltage from being applied by the output terminal to downstream powered circuitry.

In order to more particularly define the circuitry and functionality of the present invention, each of independent Claims 1, 5 and 10 has been amended to underscore the fact that the present invention monitors the voltage at the common node. In response to the voltage at the common node reaching a value associated with the onset of an over-voltage condition, a by-pass of that voltage is provided (by way of the lower FET) so that an over-voltage will not be delivered to downstream circuitry.

When comparing (or more correctly contrasting) what is defined in applicants' claims with what is disclosed in the patent to Holt et al 6,731,486, a fundamental difference becomes immediately apparent.

This difference resides in the fact that the circuitry of Holt et al monitors the regulated output voltage VFB at the circuit's output voltage port 104. This output voltage is coupled to a voltage protection circuit 220, which controllably supplies an over-voltage signal 211 through an OR gate 230 to the control input of lower FET 120 when an over-voltage condition occurs, as described in Column 3, Lines 9-42. By monitoring the output terminal, the patentees wait for the over-voltage condition to occur and then take steps to remove it.

In contrast thereto, applicants' invention does not monitor the output terminal for the presence of an over-voltage condition. Instead, applicants' circuitry and methodology monitors the common node. If the voltage at the common node reaches a value associated with the onset of an over-voltage condition, the invention immediately turns on the lower FET, so as to by-pass the common node voltage to ground, and away from the output terminal and downstream circuitry connected thereto.

To emphasize this difference, each of independent Claims 1, 5 and 10 has been amended to recite that it is the voltage at the common terminal which is monitored for the onset of an over-voltage condition associated with a short through the first switch, and it is the onset of an over-voltage condition at the common node which is used to trigger the turn on of the second switching device, so as to provide a by-pass path therethrough from the common node and thereby prevent the application of an over-voltage to downstream circuitry.

As pointed out above, in contrast to the monitoring of the voltage at the common node by the present invention, the circuit of Holt et al monitors the output voltage VFB at the output port 104. By monitoring the output node, the circuit of Holt et al waits for an overvoltage condition to occur and than turns on a lower FET 120. Applicants' claimed invention, on the other hand, monitors the common node for the onset of an overvoltage condition and, when that onset is detected, turns on the lower FET, so that an over-voltage condition will not occur. Simply put, applicants' invention prevents an over-voltage condition from occurring, whereas the circuitry of Holt et al allows an over-voltage condition to occur, and then takes steps to remove it.

Newly added Claims 15-27 are also believed to be patentable for the reasons discussed above. Moreover, Claims 15, 16 and 17 depend upon respective Claims 4, 9 and 14, which have been indicated to be directed to allowable subject matter. Consequently, Claims 15, 16 and 17 are believed to be allowable also. These claims more particularly define the controlled turn off of the upper and lower predriver MOSFETS, as described in paragraph [00017] of the specification.

Claims 18-27 particularly recite the fact that the present invention provides a by-pass current flow path from the common node to the second voltage terminal without monitoring the voltage of the output node, but rather detecting a short circuit through the first switching device between the first power supply terminal and the common node. As pointed out above, this is in contradistinction to the circuit described in the patent to Holt et al, which monitors the voltage at the output node 104, not the common node. Consequently, Claims 18-27 are also believed to be patentable.

In view of the manner in which the application has been amended to eliminate the indefiniteness raised in the outstanding

Office Action and to more particularly characterize applicants' invention, in a manner which is neither taught nor suggested by the cited prior art patent to Holt et al, favorable reconsideration of this application and a Notice of Allowability of Claims 1-27 are respectfully requested.

Finally, enclosed please find a substitute sheet of drawings for Figure 1, in which the reference numeral 10 for the upper resistor has been replaced by the reference numeral 12. This avoids duplicity with the reference numeral 10 for the control circuit of Figure 2.

Should any minor informalities need to be addressed, the Examiner is encouraged to contact the undersigned attorney at the telephone number listed below.

Please charge any shortage in fees due in connection with the filing of this paper, including Extension of Time fees, to Deposit Account No. 01-0484 and please credit any excess fees to such deposit account.

Respectfully submitted,

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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: M/S Amendment, Commissioner for Patents, P. O. Box 1450, Alexandria, VA 22313-1450, on this 30 day of September, 2004.

Murphy

In re Patent Application of:
DEQUINA ET AL
Serial No. **10/685314**
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In the Drawings:

Attached is replacement drawing sheet 1/4 which correctly identifies label 12.